



# UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE  
United States Patent and Trademark Office  
Address: COMMISSIONER FOR PATENTS  
P.O. Box 1450  
Alexandria, Virginia 22313-1450  
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/509,598	09/28/2004	Erik Petrus Antonius Maria Bakkers	NL02 0286 US	8354

24738 7590 10/23/2007  
PHILIPS ELECTRONICS NORTH AMERICA CORPORATION  
INTELLECTUAL PROPERTY & STANDARDS  
370 W. TRIMBLE ROAD MS 91/MG  
SAN JOSE, CA 95131

EXAMINER
----------

SUCH, MATTHEW W

ART UNIT	PAPER NUMBER
----------	--------------

2891

MAIL DATE	DELIVERY MODE
-----------	---------------

10/23/2007

PAPER

**Please find below and/or attached an Office communication concerning this application or proceeding.**

The time period for reply, if any, is set in the attached communication.

# Office Action Summary

Application No.

10/509,598

Applicant(s)

BAKKERS, ERIK PETRUS  
ANTONIUS MARIA

Examiner

Matthew W. Such

Art Unit

2891

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

## Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

## Status

- 1) ☒ Responsive to communication(s) filed on 11 May 2007.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

## Disposition of Claims

- 4) ☒ Claim(s) 2-5 and 14-26 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 2-5 and 14-26 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

## Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on \_\_\_\_\_ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

## Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some \* c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- \* See the attached detailed Office action for a list of the certified copies not received.

## Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☐ Information Disclosure Statement(s) (PTO/SB/08)  
Paper No(s)/Mail Date \_\_\_\_\_
- 4) ☐ Interview Summary (PTO-413)  
Paper No(s)/Mail Date. \_\_\_\_\_
- 5) ☐ Notice of Informal Patent Application
- 6) ☐ Other: \_\_\_\_\_

## DETAILED ACTION

### *Claim Rejections - 35 USC § 102*

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2. Claims 2-3, 14-15, 17-20 and 23-25 are rejected under 35 U.S.C. 102(b) as being anticipated by Le Mehaute ('037). Le Mehaute teaches an optoelectronic device (Title; Abstract; Col. 1, Lines 5) of a first electrode (Elements 4, 6) and a second electrode (Elements 5, 7) connected by a nanowire with a first region and a third region (Element 3 on either side of Element 9) each comprising a metallic material, such as gold-palladium (Col. 1, Lines 66-68; Col. 2, Lines 44-45) and having quantization effects, since the nanowire is a quantum wire (Col. 2, Line 46). The quantum wire can also be made of a semiconductor, such as doped silicon or GaAs, for example (Col. 2, Lines 1-2). The Examiner notes that the manner in which the claim is written does not limit what “quantization effects” are, so any structure capable of any quantum behavior meets the claim. A second region (Elements 8, 9) comprising a semiconductor material, such as GaAs or CdS or organics (Col. 1, Lines 15-24, 51-55; Col. 4, Lines 38-43). The device can have more than one semiconductor material, such as a doped silicon quantum

Art Unit: 2891

wire region (Element 3; Col. 2, Line 1) and a GaAs photosensitive material region (Element 8, 9; Col. 1, Lines 15-24, 51-55; Col. 4, Lines 38-43). The diameter of the second region is greater than the diameter of both the first region and the third region (see Fig. 1, for example). The length of the second region can be 100 Angstroms, for example, or 10 nanometers. The first region and the third region can have a diameter of 20 Angstroms, for example, or 2 nanometers (Col. 1, Line 60, for example).

3. Claims 14-18 rejected under 35 U.S.C. 102(e) as being anticipated by Williams ('249). Williams teaches a devices with a first electrode (Element 3 or 81, for example) and a second electrode (Element 4 or 82, for example) connected by a nanowire made of more than one semiconductor material, such as silicon germanium (Para. 0063) and comprising a first region and a third region (Elements 8 and 9, 83 and 84 or Elements 8 and 7, 84 and 85, at least) each having quantization effects, such as tunneling (Para. 0022, 0064; Figs. 3-5 and 11, 13, for example). The Examiner notes that the manner in which the claim is written does not limit what "quantization effects" are, so any structure capable of any quantum behavior meets the claim. A second region (Elements 11 or 10, 80 or 86, at least) adjoins the first and third regions. The second region has a length less than 100 nanometers, for example 60 nanometers (Para. 0060; second regions are circular) and has a diameter greater than the first and third regions (see relationship between Elements W1, W2 versus Element w; Para. 0060). The device has a first gate (Element 5<sub>1</sub> or 90) and a second gate (Element 5<sub>2</sub> or 92) and a perpendicular projection of the first gate overlaps the second region. The Examiner notes that the claim as written does not define how a perpendicular direction is defined, nor how a projection of a perpendicular

Art Unit: 2891

projection distinguishes the structural location of the first gate to the second region since any direction can be arbitrarily defined as perpendicular and also that a plan view is a perpendicular direction. The device is an optoelectronic device (Para. 0030, for example) since a laser is used with the device.

***Claim Rejections - 35 USC § 103***

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

5. Claims 5 and 22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Le Mehaute ('037) in view of Sze (Physics of Semiconductor Devices).

Le Mehaute teaches an optoelectronic device and that the first region can be doped silicon, for example (Col. 2, Lines 1-2) and the second region can also be a semiconductor, but does not teach that the first region is n-type doped and the second region is p-type doped.

Sze teaches optoelectronic devices with p-n junctions formed at the interface of an n-type doped first region and a p-type doped second region, forming an avalanche device (Pages 772-783). It would have been obvious to one of ordinary skill in the art at the time the invention was made to dope the first region of Le Mehaute n-type and the second region p-type in order to provide an avalanche device and increase the quantum efficiency of the optoelectronic device.

6. Claims 4 and 21 are rejected under 35 U.S.C. 103(a) as being unpatentable over Williams ('249) in view of McCarthy ('070).

Williams teaches a nanowire device and second region can have a diameter of, for example, 60 nanometers (Para. 0060, for example), which quantum confinement in the second region, but does not teach that the second region can have a maximum diameter of 50 nanometers.

McCarthy teaches quantum confinement in nanoparticles (Col. 10, Lines 18-21), and the diameter of the particle is dependent on the de Broglie wavelength of the carriers to be confined. McCarthy further teaches that the confinement dimension should be, for example 20 nanometers, in order to confine charge carriers at room temperature and that larger confinement dimensions require cooler than room temperature environments (Col. 6, Lines 19-29). It would have been obvious to one of ordinary skill in the art at the time the invention was made to set the maximum diameter of the second region (charge carrier confinement region) of the device of Williams to, for example, 20 nanometers, in order to achieve carrier confinement at room temperature and produce a room temperature operable device. It has been held that where the general conditions of a claim are disclosed in prior art, discovering the optimum or working ranges involves only routine skill in the art. *In re Aller*, 105 USPQ 233.

7. Claims 4, 21 and 26 are rejected under 35 U.S.C. 103(a) as being unpatentable over Le Mehaute ('037) in view of Fafard ('055).

Art Unit: 2891

Le Mehaute teaches the length of the second region and teaches that the diameter is greater than the diameter of the first region and the third region, but does not specify the diameter of the second region, which is a photosensitive material.

Fafard teaches making optoelectronic devices with photosensitive quantum dots of, for example, 200 Angstroms, or 20 nanometers (Para. 0005-0006, 0010). It would have been obvious to one of ordinary skill in the art at the time the invention was made to set the maximum diameter of the second region (photosensitive region) of Le Maute to, for example, 20 nanometers, in order to achieve three dimensional confinement and produce an optoelectronic device sensitive at normal incidence as well as having a broader wavelength range sensitivity, including infrared (Fafard Para. 0005-0006). It has been held that where the general conditions of a claim are disclosed in prior art, discovering the optimum or working ranges involves only routine skill in the art. *In re Aller*, 105 USPQ 233.

### ***Response to Arguments***

8. Applicant's arguments with respect to claims 2-5 and 14-26 have been considered but are moot in view of the new ground(s) of rejection.

### ***Conclusion***

9. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure:

Art Unit: 2891

- i. Higurashi ('961) teaches a quantized nanowire device (Fig. 1);
- ii. Nakajima ('157) teaches a quantized transistor device (Figs. 4A, 8);
- iii. Lee ('734) teaches NPN nanowire transistors;
- iv. Takahashi ('154) teaches a nanowires with a wide center (Figs. 14-15);
- v. Fraboulet ('310) teaches a single electron transistor;
- vi. Katah ('790) teaches quantum confined optoelectronic devices (Figs. 1-6);
- vii. Penner ('902) teaches methods of producing nanowires;
- viii. Lux (H1570) teaches quantum confined transistor structures (Figs. 1-2);
- ix. Dobson ('954) teaches nanowire light emitting devices (Figs. 5-6);
- x. Hirai ('140) teaches resonant electron transfer devices with wider regions and narrower regions (Figs. 2-3);
- xi. Dutta ('194) teaches nanowires with wider center regions and narrower peripheral regions (Figs. 3-4);
- xii. Morimoto ('744) teaches nanowire-based quantum effect devices;
- xiii. Fraboulet ('539) teaches quantum confinement based transistors;
- xiv. Ilyanok ('224) teaches nanowire devices with wider dots (Figures);
- xv. Sugiyama ('432) teaches quantum transistors (Figs. 20-24).

10. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).



Art Unit: 2891

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

#### ***Contact Information***

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Matthew W. Such whose telephone number is (571) 272-8895. The examiner can normally be reached on Monday - Friday 9AM-5PM EST.

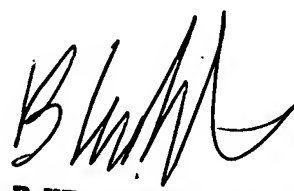
If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Bradley W. Baumeister can be reached on (571) 272-1722. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Art Unit: 2891

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Matthew W. Such  
Examiner  
Art Unit 2891

MWS  
10/19/07

  
**B. WILLIAM BAUMEISTER**  
**SUPERVISORY PATENT EXAMINER**  
**TECHNOLOGY CENTER 2800**